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2	US 20010019500		US-PGPU	20010906	39
3	US 5835406 A		USPAT	19981110	17

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Chevallier et al. [45] Date of Patent: Nov. 10, 1998

[54] APPARATUS AND METHOD FOR SELECTING DATA BITS READ FROM A MULTISTATE MEMORY

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[21] Appl. No.: 736,380

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[51] Int. Cl.[6] G11C 11/34; G11C 2/00

[52] U.S. Cl. 365/185.03; 365/168; 365/189.02; 365/230.02

[58] Field of Search 365/185.03, 189.02, 365/230.02, 205, 168

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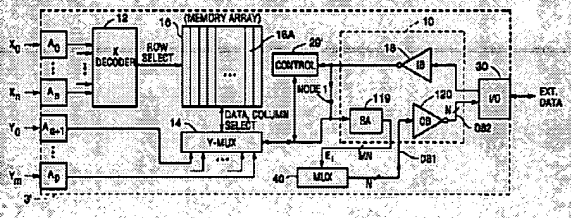
[57] ABSTRACT

An apparatus and method which sequentially selects subsets of data bits read in parallel from an array of memory cells (each cell being operated as a multistate memory device) and sequentially asserts the selected subsets to a data bus. Preferably, the cells are flash memory cells. Preferably, the apparatus includes a sense amplifier circuit, a multiplexer, and circuitry operable to read a number (N) of the cells in parallel, whether the cells are operated as binary or multistate devices. The sense amplifier has N input lines and MN output lines, where M is the number of binary bits in a binary representation of the data read from each cell operated as a multistate device. The multiplexer has MN inputs (each connected to one of the output lines of the sense amplifier circuit), N outputs connected to a data bus having N-bit width, and is controllable to output selected N-bit subsets of the MN bits received at its MN inputs. Another aspect of the invention is a memory system including such a multiplexer and read/write circuitry operable in a mode in which it writes data to selected cells of the array (leaving each cell in an erased or programmed state) or reads a binary data bit from each of N selected cells, where the read/write circuitry is also operable in another mode in which it writes data to selected cells of the array (leaving each cell in an erased state or a selected one of two or more possible programmed states) or reads data (indicative of an ordered set of at least two binary data bits) from each of N selected cells.

33 Claims, 6 Drawing Sheets



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